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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,471	01/18/2002	Seungyoon P. Song	1779CIP	6513

7590 03/27/2003

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,471	SONG, SEUNGYOON P.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,348,812. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations are similar.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Kondou et al (4,876,466).

Regarding claim 1, Kondou shows a dynamic (dynamic type, col. 6, lines 14-19) programmable logic array comprising:

At least one logic plane (AND PLANE, Fig. 3A); and

At least one reprogrammable evaluate module (200) within the at least one logic plane, the at least one reprogrammable evaluate module (Fig. 4B, 5A) including a first program input (B), a second program input (a or W), a storage element (Fig. 5A) coupled to the first and second program inputs, and input pass transistor (202, Fig. 4A; Figure 6 shows 202 transistor) coupled to the output of storage element and an evaluate transistor (100, Fig. 4B) coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

Regarding claim 2, Kondou shows the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input (d) and a gate of the evaluate transistor (see Fig. 4A, 5A, & 6).

Regarding claim 3, Kondou shows the storage element comprises a multiple transistor register.

Regarding claim 4, Kondou shows the multiple transistor register comprises:

A program data pass transistor, which includes a gate source and drain, the source (B, Fig. 5A) of the program data pass transistor is coupled to the first program input and the gate is coupled to the second program input (W);

A first inverter (a top inverter, Fig. 5) whose input is coupled to the drain of the program data pass transistor and whose output is coupled to the output of the storage element; and

A second inverter (a bottom inverter) whose input is coupled to the output of the first inverter and whose output is coupled to the input of the first inverter, wherein the storage element is written by placing a desired value on the first program input and asserting the second program input.

Regarding claim 8, Kondou shows a dynamic programmable logic array (Fig. 3A) comprising:

A first logic plane (AND PLANE);

A first reprogrammable evaluate module (200) with the first logic plane;

A second logic plane (OR PLANE) coupled to the first logic plane and for providing an output (O); and

A second reprogrammable evaluate module (200) within the second logic plane, wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

The limitations of claims 9-17are rejected as above claims.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Hanrahan et al (6,311,200).

Regarding claim 1, Hanrahan shows a dynamic programmable logic array comprising:

At least one logic plane (24, Fig. 1); and

At least one reprogrammable evaluate module (76, Fig. 3) within the at least one logic plane, the at least one reprogrammable evaluate module including a first program input (DATA INPUT, Fig. 7), a second program input (WRITE SELECT), a storage element (NOR-gate and inverter) coupled to the first and second program inputs, and input pass transistor (82) coupled to the output of storage element and an evaluate transistor (84) coupled to the input pass transistor, wherein the storage element comprises at least one of SRAM cell (SRAM cell), FLASH memory cell, fuse, anti-fuse, ferroelectric memory cell, EEPROM cell, and EPROM cell.

Regarding claim 2, Hanrahan shows the at least one programmable evaluate module includes the first program input, the second program input, and the storage element coupled to the first and second program inputs, and the input pass transistor, the input pass transistor including a gate, source and drain, wherein the gate is coupled to the output of the storage element and the source and the drain are coupled to a control input and a gate of the evaluate transistor (see Fig. 3).

Regarding claim 3, Hanrahan shows the storage element comprises a multiple transistor register (transistors are inherent elements from NOR-gate and inverter).

Regarding claim 5, Hanrahan shows an evaluate disable transistor (86) which includes a gate, source and drain, the gate is coupled to the output of the storage element, the source is coupled to the gate of the evaluate transistor, and the drain is coupled to the ground; and the output of the storage element turns on one of the input pass transistor or the evaluate disable transistor at any given time.

The limitations of claims 14-15, and 18 are rejected as above claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
March 17, 2003